AMENDMENTS TO THE CLAIMS:

Please amend the claims as follows, substituting any amended claim(s) for the corresponding pending claim(s):

Claims 1-16. (Canceled)

17. (Withdrawn) A method of fabricating a portion of a semiconductor device comprising:

forming a gate structure on a substrate by:

forming an insulating oxide layer on the substrate;

depositing a nitride layer on the oxide layer; and

depositing a polysilicon layer on the nitride layer; and

reoxidizing the polysilicon layer within the gate structure to form a layer of oxide over the gate structure and to cause an uplift in portions of the nitride layer proximate a peripheral edge of the gate structure,

wherein asperities are absent from a bottom surface of the polysilicon layer.

18. (Withdrawn) The method of claim 17, wherein the depositing step includes depositing the nitride layer on the insulating oxide layer to a thickness from about 10 Å to about 50 Å.

19. (Withdrawn) The method of claim 17, wherein the reoxidizing step includes reoxidizing the gate structure to form an oxide layer from about 25 Å to about 500 Å thick.

20. (Withdrawn) The method of claim 17, further comprising:

patterning the gate structure by selectively etching away portions of the insulating oxide, nitride and polysilicon layers to expose a portion of the substrate and form a peripheral edge around the gate structure; and

exposing the substrate to an oxidizing ambient during reoxidation to oxidize the exposed portion of the substrate and the polysilicon layer within the gate structure.

21. (Withdrawn) The method of claim 20, wherein the reoxidation grows the oxide layer below the peripheral portion of the nitride layer.

22. (Withdrawn) The method of claim 20, wherein the reoxidation causes an indentation in the substrate near the peripheral edge of the gate structure.

23. (Withdrawn) The method of claim 17, further comprising:

prior to the reoxidizing step, forming source and drain regions in the substrate.

24. (Canceled)

25. (Withdrawn) A method for fabricating a portion of a semiconductor device, comprising:

forming an oxide gate layer on a surface of a substrate;

forming a nitride layer on the oxide gate layer by depositing the nitride layer on the oxide gate layer;

forming a polysilicon layer on the nitride layer;

patterning the polysilicon and nitride layers to form a gate structure; and

reoxidizing the polysilicon layer within the gate structure to

form a layer of oxide over the gate structure and on sidewalls of the polysilicon layer,

grow the oxide layer beneath a peripheral region of the nitride layer thicker, causing an uplift in the peripheral region of the nitride layer, and

prevent formation of asperities from an interface between the polysilicon layer and the nitride layer.

Claims 26-45 (Canceled)

46. (Currently Amended) An integrated circuit device comprising:

a substrate;

a gate structure, wherein the gate structure includes:

a gate oxide layer on the substrate,

a nitride layer on and directly contacting the gate oxide layer, and

a polysilicon layer over the nitride layer;

a channel region under the gate structure; and

source/drain regions in the substrate adjacent the channel region,

wherein the gate structure has a peripheral edge and further including an uplift in portions of the nitride layer proximate the peripheral edge of the gate structure, the uplift caused by reoxidation of the polysilicon layer within the gate structure to increase an electric field during operation at the peripheral edge, wherein asperities are absent from a bottom surface of the polysilicon layer and a thickness of an oxidation layer produced by said reoxidation is from about 25 Å to about 500 Å on said substrate.

47. (Original) The integrated circuit device of claim 46, wherein the nitride layer is from about 10 Å to about 50 Å thick.

48. (Original) The integrated circuit device of claim 46, wherein the nitride layer is deposited over said gate oxide layer.

49. (Original) The integrated circuit device of claim 46, wherein the nitride layer is formed by nitrogen implantation to form an implanted area and by annealing of the implanted area.

50. (Canceled)

51. (Previously Presented) The integrated circuit device of claim 46, wherein the substrate has a surface and further including an indentation in the surface of the substrate located proximate to the peripheral edge of the gate structure, the indentation resulting from reoxidation of the gate structure.

52. (Previously Presented) The integrated circuit device of claim 46 further wherein the gate structure includes sidewall spacers located on each edge of the gate structure and lightly doped drain regions in the substrate below the sidewalls spacers.

53. (Original) The integrated circuit device of claim 46, wherein the substrate is a p-type substrate and wherein the source/drain regions are formed by implanting n-type impurities in the p-type substrate.

54. (Previously Presented) The integrated circuit device of claim 51, wherein the source/drain regions are implanted prior to reoxidation.

55. (Previously Presented) The integrated circuit device of claim 53, wherein the source/drain regions are implanted after reoxidation.

56. (Previously Presented) The integrated circuit device of claim 46, wherein the channel region has a length not greater than 0.8 μm.

57. (Previously Presented) The integrated circuit device of claim 46, wherein the gate oxide layer is not greater than 200 Å thick.

58. (Withdrawn) The method of claim 23, wherein a channel region beneath the gate structure between the source/drain regions has a length not greater than 0.8 μm.

59. (Withdrawn) The method of claim 25, further comprising:

forming the oxide gate layer to a thickness not greater than 200 Å.